a gate insulating film provided between the channel region and the gate electrode;

a source-drain region connected to said channel region;

a source-drain wiring layer electrically connected to said source-drain region;

a gate wiring layer electrically connected to said gate electrode,

comprising a extension extending outwardly from a part of at least one of the

gate wiring layer and the source-drain wiring layer, the part being defined by two contact

holes with which another contact hole is aligned .--

--45. The thin film transistor according to claim 44, an extension of the gate electrode extending outwardly provided above the channel being formed.--

--46. The thin film transistor according to claim 44, an extension of the channel region extending outwardly therefrom being formed.--

REMARKS

Claims 25-46 are pending. By this Amendment, claims 1-4, 7 and 9-24 are cancelled. Claims 25-46 are added. Reconsideration of the above amendments and following remarks is respectfully requested.

I. CLAIMS 1-4, 7, 9-21 AND 24 SATISFY THE REQUIREMENTS OF 35 §112, SECOND PARAGRAPH

The Office Action rejects claims 1-4, 7, 9-21 and 24 under 35 U.S.C. §112, second paragraph, as indefinite. Claims 1-4, 7, 9-21 and 24 are cancelled. Withdrawal of the rejection under 35 U.S.C., second paragraph, is respectfully requested.

II. CLAIMS 1-4, 7, 9-21 AND 23 SATISFY THE REQUIREMENTS OF 35 U.S.C. § 112, FIRST PARAGRAPH

The Office Action rejects claimS 1-4, 7, 9-21 and 23 under 35 U.S.C. §112, first paragraph, as containing subject matter not described in the specification. Claims 1-4, 7, 9-21

and 23 are cancelled. Withdrawal of the rejection under 35 U.S.C. §112, first paragraph, is respectfully requested.

III. THE CLAIMS DEFINE ALLOWABLE SUBJECT MATTER

The Office Action rejects claims 1 and 14-17 under 35 U.S.C. §102(e) as being anticipated by U.S. Patent No. 5,616,935 to Koyama et al; claims 1-3, 7, 8 and 17 under 35 U.S.C. § 102(e) as unpatentable over U.S. Patent No. 5,623,155 to Kerber et al; claims 1-3, 9, 14 and 17 under 35 U.S.C. § 102(e) as unpatentable over U.S. Patent No. 5,920,085 to Han et al.; claims 1, 9, 15 and 16 under 35 U.S.C. § 102(e) as unpatentable over Yamazaki et al.; and claims 1-3, 14 and 17 under 35 U.S.C 102(e) over U.S. Patent No. 6,064,090 to Miyamoto et al.

Koyama et al. does not teach "wherein an extension of the channel region extending outwardly therefrom is formed", as claimed in claim 26. Nor does Koyama teach or disclose "an extension of the gate electrode extending outwardly provided above the channel region is formed" as claimed in claim 25 or "a extension extending outwardly from a part of at least one of the gate wiring layer and the source-drain wiring layer, the part being defined by two contact holes with which another contact hole is aligned", as claimed in claim 44.

Instead, Koyama teaches making one channel length shorter than another channel length can reduce the threshold voltage required in a thin film transistor (TFT).

Because Koyama does not disclose the features of the claimed invention, it cannot provide the advantages of the claimed invention. For example, Koyama discloses the channel length of a P-channel TFT made shorter than that of an N-channel TFT, preferably by 20%, column 2 lines 23-36. Thus, Koyama does not provide the advantage of a portion extending from the channel region which will further help to dissipate heat during operation.

However, Koyama is completely devoid of this advantage. The fact that Koyama is completely devoid of this advantage shows that it would not have been obvious to one of

ordinary skill in the art to modify its disclosure to make up for the deficiencies in Koyama discussed above. Specifically, if it had been obvious to one of ordinary skill in the art to modify Koyama to make up for the deficiencies discussed above, then one of ordinary skill in the art would have done so to attain the advantages. However, no such disclosures have been found that show the claimed invention.

For at least these reasons, at least claims 25, 26 and 44 are not anticipated by Koyama.

Similarly, Kerber does not teach "wherein an extension of the channel region extending outwardly therefrom is formed", as claimed in claim 26. Nor does Kerber teach or disclose "an extension of the gate electrode extending outwardly provided above the channel region is formed" as claimed in claim 25 or "a extension extending outwardly from a part of at least one of the gate wiring layer and the source-drain wiring layer, the part being defined by two contact holes with which another contact hole is aligned", as claimed in claim 44.

Instead, Kerber et al. teaches in col. 1, lines 64-col. 2, line 1 that "one end of the ridge does not project beyond, or only slightly projects beyond, the channel region. Undesirable, additional capacitances between the gate electrode and the source and drain regions are thus kept optimally small." Thus, Kerber et al. teach away from "an extension of the channel region extending outwardly therefrom", as claimed in claim 26.

Accordingly, at least claims 25, 26 and 44 are not anticipated by Kerber. Withdrawal of the rejections of at least claims 25, 26 and 44 under 35 U.S.C. §102(e) is respectfully requested.

Similarly, Han does not teach or disclose "wherein an extension of the channel region extending outwardly therefrom is formed", as claimed in claim 26. Nor does Han teach or disclose "an extension of the gate electrode extending outwardly provided above the channel region is formed" as claimed in claim 25 or "a extension extending outwardly from a part of at

least one of the gate wiring layer and the source-drain wiring layer, the part being defined by two contact holes with which another contact hole is aligned", as claimed in claim 44.

Instead, Han et al. teaches a method for forming a field effect transistors which are capable of high saturation current and low leakage current, which may only require a single implantation step and which may be formed in a self-lined manner to provide a symmetrical transistor. Han et al. does not teach anything about a "an extension of the channel region extending outwardly therefrom", as claimed in claim 26.

Accordingly, at least claims 25, 26 and 44 are not anticipated by Han. Withdrawal of the rejection of at least claims 25, 26 and 44 under 35 U.S.C. §102(e) is respectfully requested.

Yamazaki does not teach "wherein an extension of the channel region extending outwardly therefrom is formed ", as claimed in claim 26. Nor does Yamazaki teach or disclose "an extension of the gate electrode extending outwardly provided above the channel region is formed" as claimed in claim 25 or "a extension extending outwardly from a part of at least one of the gate wiring layer and the source-drain wiring layer, the part being defined by two contact holes with which another contact hole is aligned", as claimed in claim 44.

Instead, Yamazaki et al. teaches a thin film transistor which is not effected by crystal grain boundaries. Yamazaki et al. does not teach or anticipate "an extension of the channel region extending outwardly ", as claimed in claim 26.

Accordingly, Ymazaki does not anticipate the claimed invention. Withdrawal of the rejection 35 U.S.C. §102(e) is respectfully requested.

Miyamoto et al. does not teach or suggest " wherein an extension of the channel region extending outwardly therefrom is formed ", as claimed in claim 26. Nor does Miyamoto teach or disclose "an extension of the gate electrode extending outwardly provided above the channel region is formed" as claimed in claim 25 or "a extension extending

outwardly from a part of at least one of the gate wiring layer and the source-drain wiring layer, the part being defined by two contact holes with which another contact hole is aligned", as claimed in claim 44.

Instead, Miyamoto et al. teaches a semiconductor device having stable characteristics with suppressed source/drain leak current. Miyamoto et al. do not teach or suggest any means for wherein "a portion outwardly extending from the channel region", as claimed in claim 26.

Accordingly, is not anticipated by Miyamoto. Withdrawal of the rejection under 35 U.S.C. §102(e) is respectfully requested.

IV. CONCLUSION

In view of the foregoing remarks, Applicants respectfully submit that claims 25-46 define patentable subject matter and that the application is in condition for allowance.

Favorable consideration and prompt allowance are earnestly solicited.

Should the Examiner believe anything further is desirable in order to place this application in even better condition for allowance, the Examiner is invited to contact Applicants' undersigned representative at the telephone number listed below.

Respectfully submitted,

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Attachment: Appendix

Date: July 5, 2001

OLIFF & BERRIDGE, PLC P.O. Box 19928 Alexandria, Virginia 22320 Telephone: (703) 836-6400 DEPOSIT ACCOUNT USE
AUTHORIZATION
Please grant any extension
necessary for entry;
Charge any fee due to our
Deposit Account No. 15-0461

APPENDIX

Changes to Claims:

Claims 1-4, 7 and 9-24 are canceled.

Claims 25-46 are added.